4-channel BLT driver for CD players

BA6196FP

The BA6196FP is an IC designed CD players and has an internal 4-channel BTL driver, 5V regulator (attached PNP transistor required), standard operational amplifier and a thermal shutdown feature. The driver has gain adjustment input pins for each channel, allowing gain to be set to the desired value. Also, the internal level shift circuit helps reduce the number of attached components.

●Applications

CD players, CD-ROM drives and other optical disc devices

●Features

1) 4-channel BTL driver in a 28-pin HSOP package, for miniaturization of applications.
2) Gain is adjustable with an attached resistor.
3) Internal thermal shutdown circuit.
4) Internal 5V regulator. (required attached PNP transistor)
5) Internal standard operational amplifier.

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	18	V
Power dissipation	Pd	1700*1	mW
Operating temperature	Topr	−35~85	℃
Storage temperature	Tstg	−55~150	℃
Maximun current	$I_{O\,Max.}$	1.4*2	A

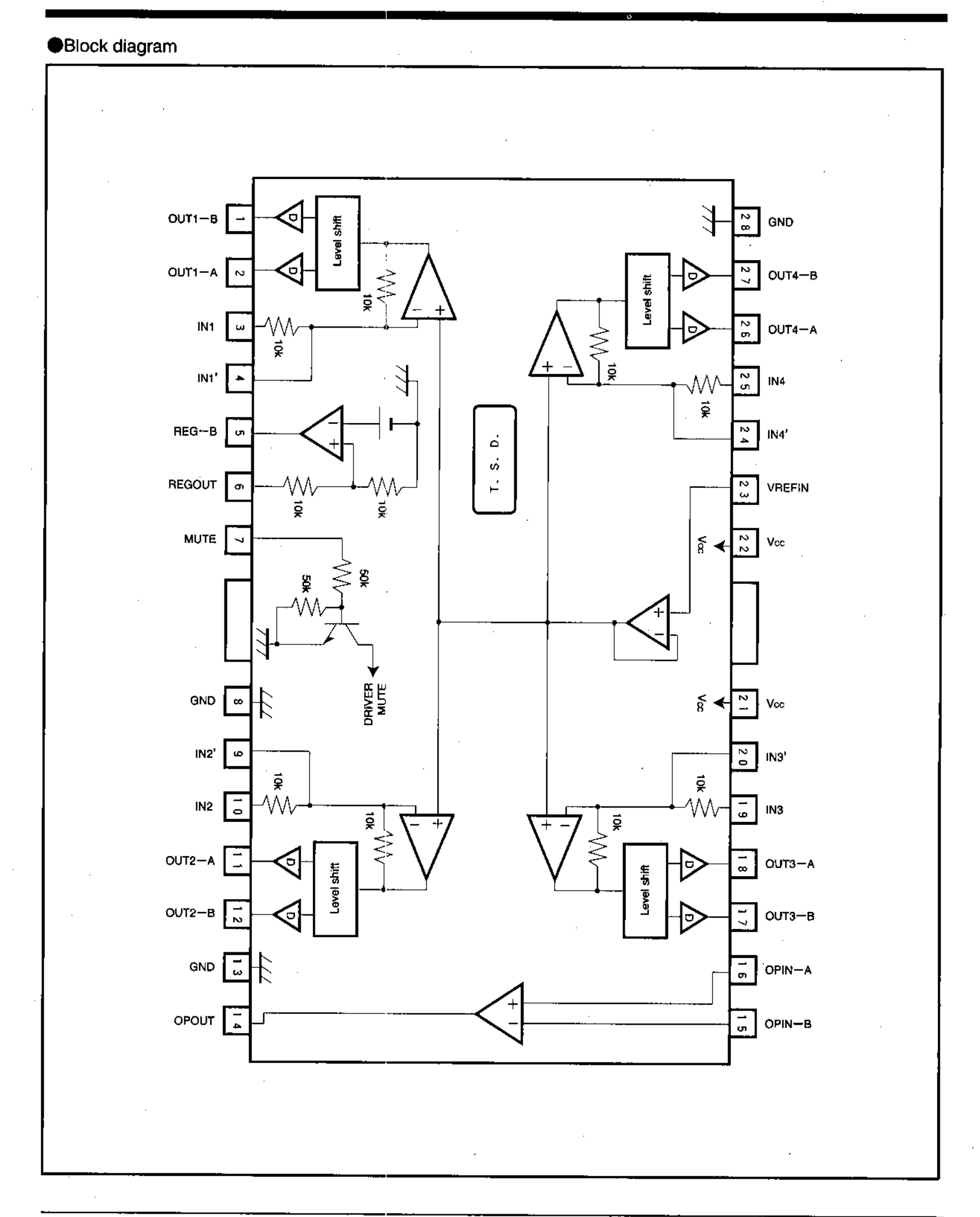
*1 When mounted to a 50 × 50 × 1.0 mm paper phenol board
Reduced by 13.6 mW for each increase in Ta of 1℃ over 25℃.
*2 Within the range of power dissipation and safe operational area (ASO)

●Recommended operating conditions (Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	6	−	12	V
		5.5	−	12	V*3

*3 Without regulator

●Block diagram

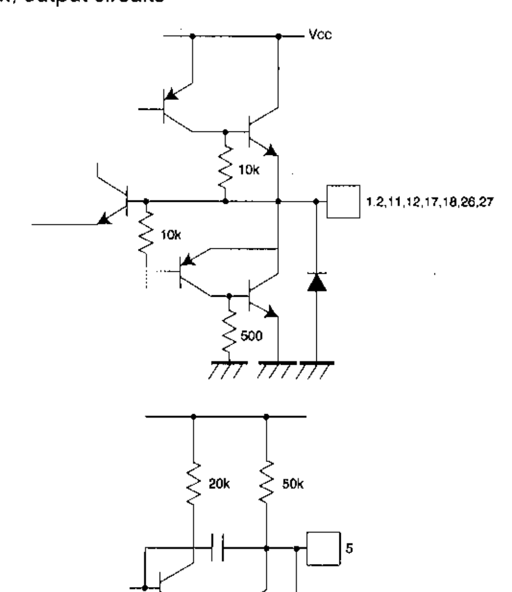


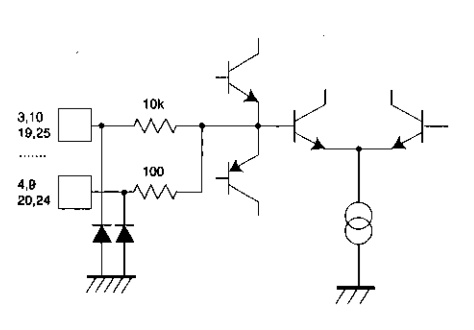
●Pin descriptions

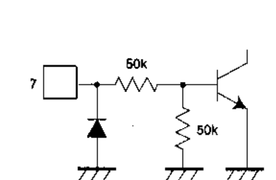
Pin No.	Pin name	Function
1	OUT1−B	Channel 1 negative output
2	OUT1−A	Channel 1 positive output
3	IN1	Channel 1 input
4	IN1'	Input for channel 1 gain adjustment
5	REG−B	Connect to base of attached regulator transistor
6	REGOUT	Connect to base of attached regulator transistor (output)
7	MUTE	Mute control
8	GND	Ground
9	IN2'	Input for channel 2 gain adjustment
10	IN2	Channel 2 input
11	OUT2−A	Channel 2 positive output
12	OUT2−B	Channel 2 negative output
13	GND	Substrate ground
14	OPOUT	Operational amplifier output
15	OPIN−B	Operational amplifier (negative) input
16	OPIN−A	Operational amplifier (positive) input
17	OUT3−B	Channel 3 negative output
18	OUT3−A	Channel 3 positive output
19	IN3	Channel 3 input
20	IN3'	Input for channel 3 gain adjustment
21	V_{CC}	Power supply
22	V_{CC}	Power supply
23	VREFIN	Reference amplifier input (bias)
24	IN4'	Input for channel 4 gain adjustment
25	IN4	Channel 4 input
26	OUT4−A	Channel 4 positive output
27	OUT4−B	Channel 4 negative output
28	GND	Substrate ground

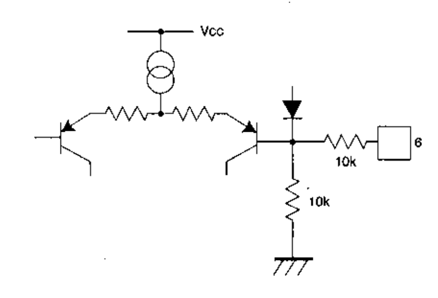
Note : "Positive input" and "negative input" indicate polarity relative to input:
HIGH input → positive output (HIGH), negative output (LOW).

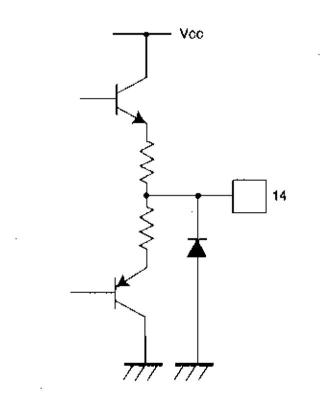
●Input / output circuits

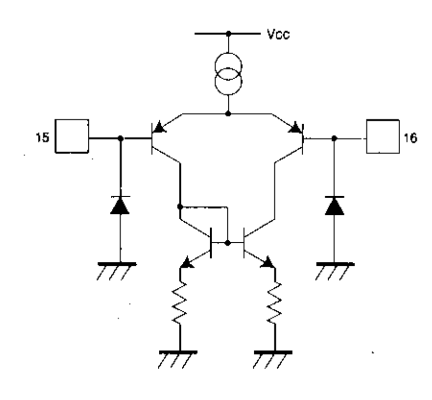


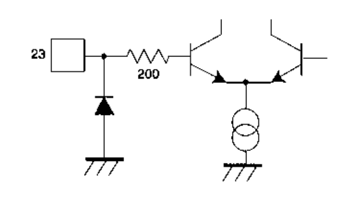












Vcc
15
16

●Electrical characteristics (unless otherwise noted, Ta=25℃, V_{CC}=8V, f=1kHz, R_L=8Ω)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
Quiescent current	I_{CC}	5.5	9.5	13.5	mA	No load	Fig.1
Output offset voltage	V_{OO}	−30	−	30	mV		Fig.1
Maximun output amplitude	V_{OM}	2.5	3.0	−	Vrms	Vin=2Vrms, 1kHz	Fig.1
Maximun output current 1	I_{OSO}	0.5	0.8	−	A	Output = GND when Rl = 4 Ω	Fig.1
Maximun output current 2	I_{OSI}	0.5	0.8	−	A	Output = Vcc when Rl = 4 Ω	Fig.1
Closed loop voltage gain	G_{VC}	3.5	5.5	6.5	dB	Vin=0.1Vrms, 1kHz	Fig.1
Ripple rejection	RR	−	60	−	dB	Vin=0.1Vrms, 100Hz	Fig.1
Slew rate	SR	−	2.0	−	V/μS	100 Hz square wave, 3 Vp-p output	Fig.1
Mute-off voltage	V_{MOFF}	2.0	−	−	V		Fig.1
〈5 V regulator〉							
Output voltage	Vreg	4.75	5.00	5.25	V	IL=100mA	Fig.1
Output load variation	ΔV_{RL}	−50	0	10	mV	IL=0~200mA	Fig.1
Supply voltage variation	ΔVVCC	−10	0	25	mV	(V_{CC}=6~9V) IL=100mA	Fig.1
〈Operational amplifier〉							
Offset voltage	V_{OFOP}	−5	0	5	mV		Fig.1
Input bias current	I_{BIAS}	−	−	300	nA		Fig.1
Output voltage, H level	V_{OHOP}	6.0	−	−	V		Fig.1
Output voltage, L level	V_{OLOP}	−	−	1.1	V		Fig.1
Output drive current (source)	I_{SOU}	10	40	−	mA	50Ω at GND	Fig.1
Output drive current (sink)	I_{SIN}	10	50	−	mA	50Ω at Vcc	Fig.1
Closed loop voltage gain	G_{VO}	−	78	−	dB	Vin=−75dBV, 1kHz	Fig.1
Slew rate	SR_{OP}	−	1	−	V/μS	100 Hz square wave, 4 Vp-p output	Fig.1
Ripple rejection	RR_{OP}	50	65	−	dB	Vin=0.1Vrms, 100Hz	Fig.1
Common mode rejection ratio	CMRR	70	84	−	dB	Vin=0.1Vrms, 1kHz	Fig.1

◎ Not designed for radiation resistance.

●Measurement circuit

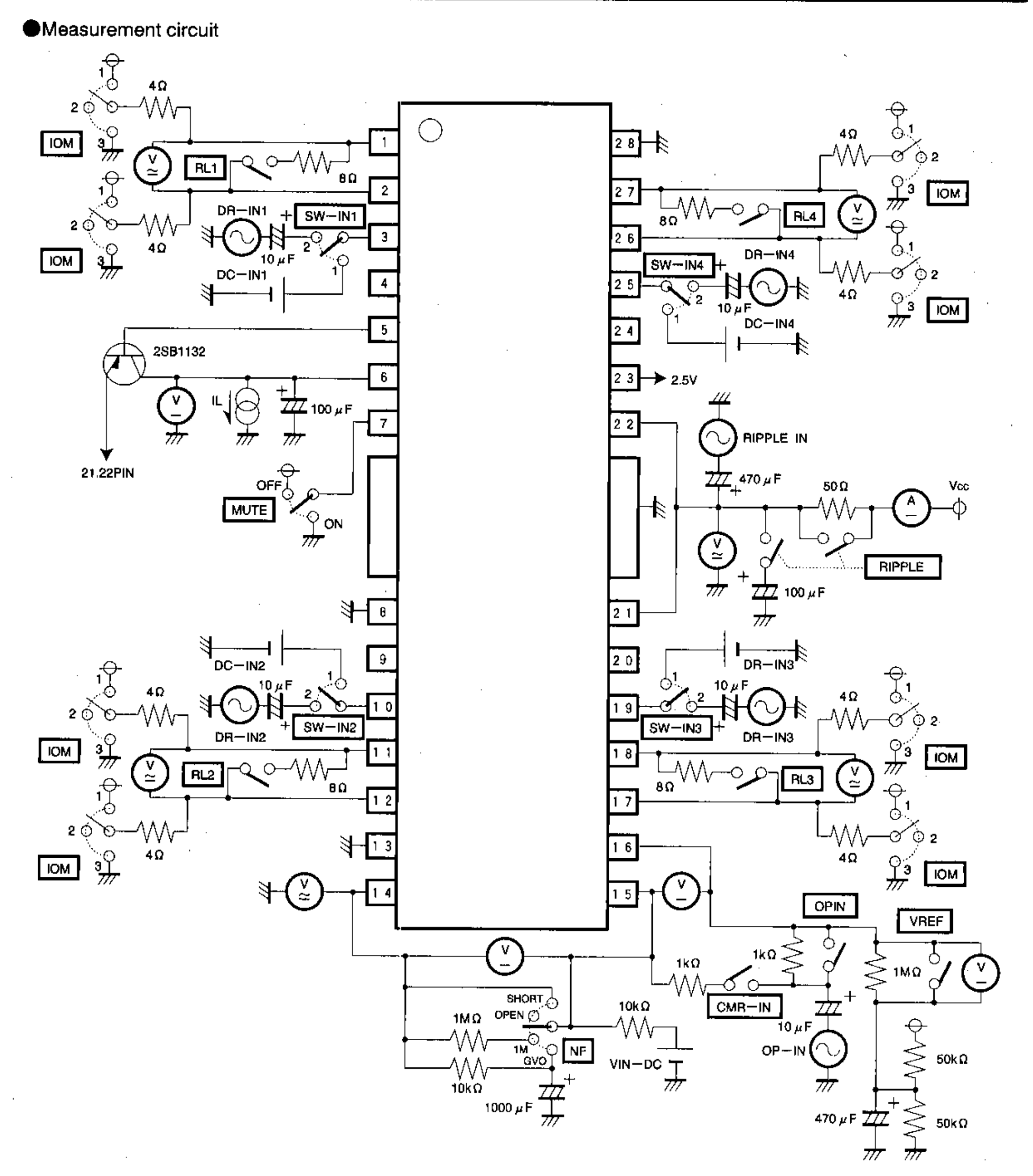


Fig. 1

●Measurement circuit switch table

Parameter	Switch										Input					Conditions
	RIPPLE	MUTE	RL	IOM	OPIN	VREF	CMR-IN	NF	OPOUT	SW−IN	DR−IN	DC−IN	RIPPLE IN	VOP IN	VIN DC	
Quiescent current	ON	OFF	OFF	2	ON	ON	OFF	SHORT	2	2	0	0	0	0	OFF	
Output offset voltage	↓	↓	ON	↓	↓	↓	↓	↓	↓	1	↓	2.5V	↓	↓	↓	
Maximun output amplitude	↓	↓	↓	↓	↓	↓	↓	↓	↓	2	2Vrms	0	↓	↓	↓	Only one channel on at a time
Maximun output current 1	↓	↓	OFF	3	↓	↓	↓	↓	↓	1	0	2.5V	↓	↓	↓	
Maximun output current 2	↓	↓	↓	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Closed loop voltage gain	↓	↓	ON	2	↓	↓	↓	↓	↓	2	0.1Vrms	0	↓	↓	↓	
Ripple rejection	OFF	↓	↓	↓	↓	↓	↓	↓	↓	1	0	2.5V	0.1Vrms	↓	↓	
Slew rate	ON	↓	↓	↓	↓	↓	↓	↓	↓	2	⎍	0	0	↓	↓	
〈Regulator〉																
Output voltage	↓	↓	OFF	↓	↓	↓	↓	↓	↓	↓	0	0	↓	↓	↓	
Output load variation	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Supply volt. variation	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
〈Operational amplifier〉																
Offset voltage	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
Input bias current	↓	↓	↓	↓	↓	OFF	↓	1M	↓	↓	↓	↓	↓	↓	↓	
Output voltage, H level	↓	↓	↓	↓	↓	ON	↓	OPEN	↓	↓	↓	↓	↓	↓	2V	
Output voltage, L level	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	6V	
Out. driver current (sink)	↓	↓	↓	↓	↓	↓	↓	SHORT	1	↓	↓	↓	↓	↓	OFF	
Out. driver current (source)	↓	↓	↓	↓	↓	↓	↓	↓	3	↓	↓	↓	↓	↓	↓	
Voltage gain (open loop)	↓	↓	↓	↓	↓	↓	↓	GVO	2	↓	↓	↓	↓	−75dBV	↓	
Slew rate	↓	↓	↓	↓	↓	↓	↓	SHORT	↓	↓	↓	↓	↓	⎍	↓	
Ripple rejection	OFF	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0.1Vrms	0	↓	
Common mode rejection ratio	ON	↓	↓	↓	OFF	ON	ON	1M	↓	↓	↓	↓	0	0.1Vrms	↓	

●Operation notes

1. The BA6196FP has an internal shutdown circuit. The output current is muted when the chip temperature exceeds 175°C (typically).
2. If the mute pin (7 pin) voltage is opened or lowered below 0.5V, the output current will be muted. The mute pin should be pulled up above 2.0V during normal use.
3. The bias pin (23 pin) is muted when lowered below 1.4V (typically). Make sure it stays above 1.6V during normal use.
4. Muting occurs during thermal shutdown, mute-on operations or a drop in the bias pin voltage. In each case, only the drivers are muted. During muting, the output pins remain at the internal bias voltage, roughly $(V_{CC}-V_F)/2$.
5. The internal circuits turn off when the supply voltage drops below 4.5V (typically), and turn on again when it rises above 4.7V (typically).
6. Be sure to connect the IC to a 0.1 μF bypass capacitor to the power supply, at the base of the IC.
7. The radiating fin is connected to the package's internal GND, but should also be connected to an external ground.
8. The capacitor between regulator output (6 pin) and GND also serves to prevent oscillation of the IC, so select one with good temperature characteristics.

●Application example

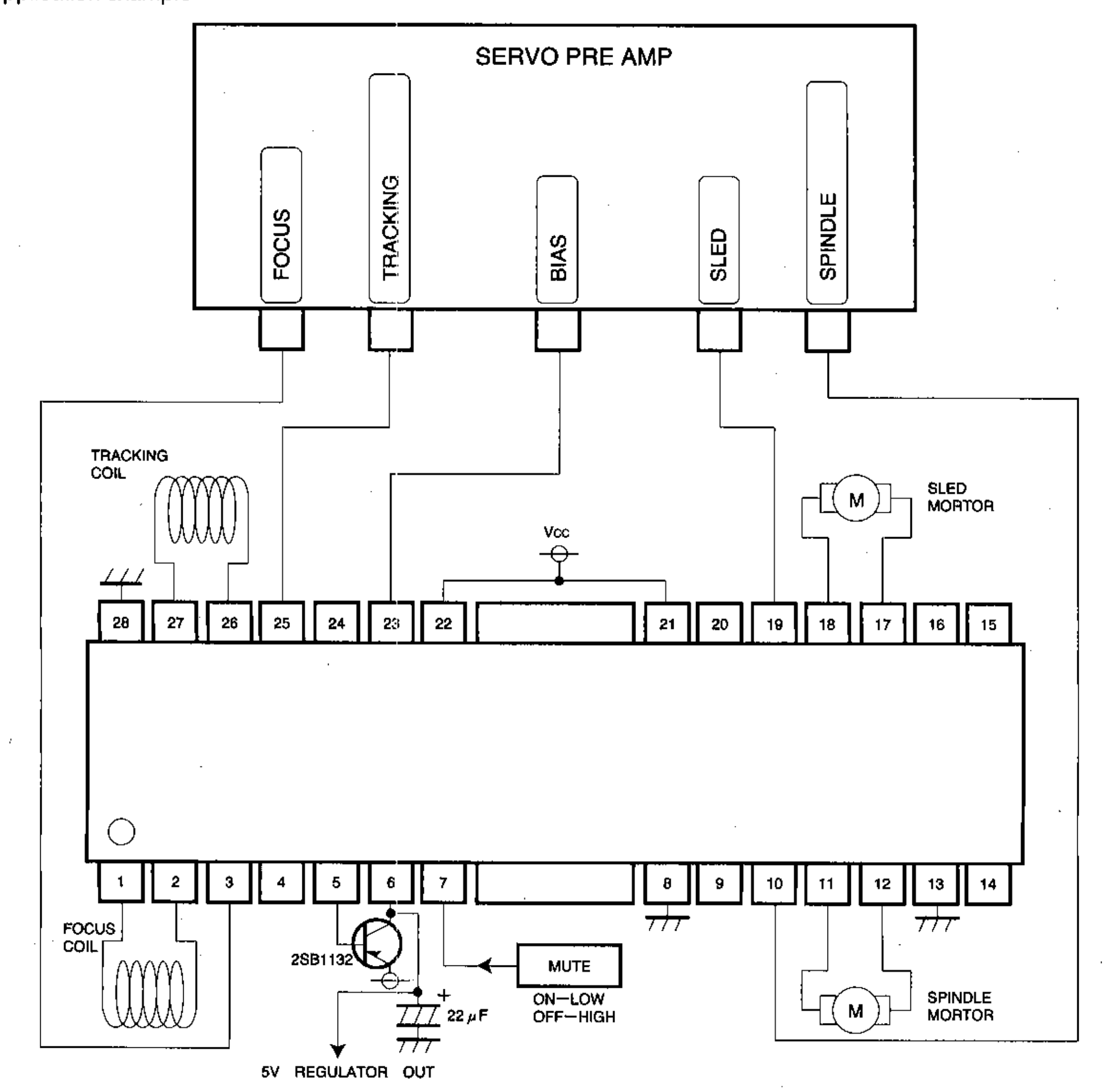


Fig. 2

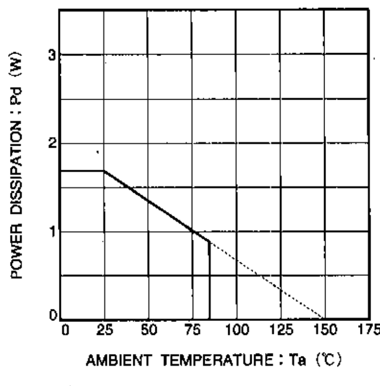


Fig. 3 Thermal derating curve

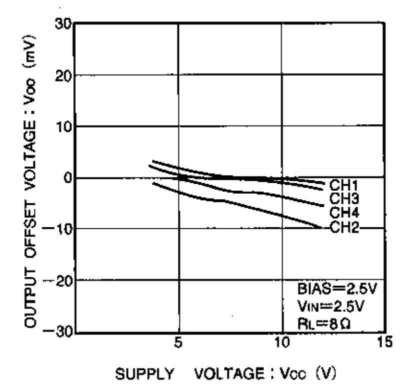


Fig. 4 Supply voltage vs. driver output offset voltage

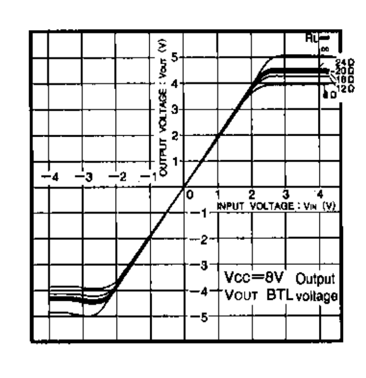


Fig. 5 I/O characteristics (variable load, Vcc = 8 V)

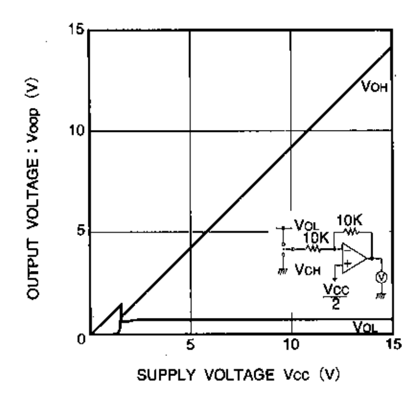


Fig. 6 Supply voltage vs. operational amplifier output voltage (high and low levels)

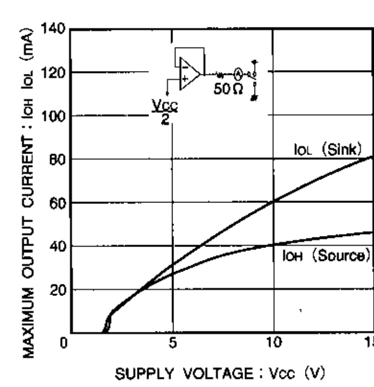


Fig. 7 Supply voltage vs. operational amplifier driver current

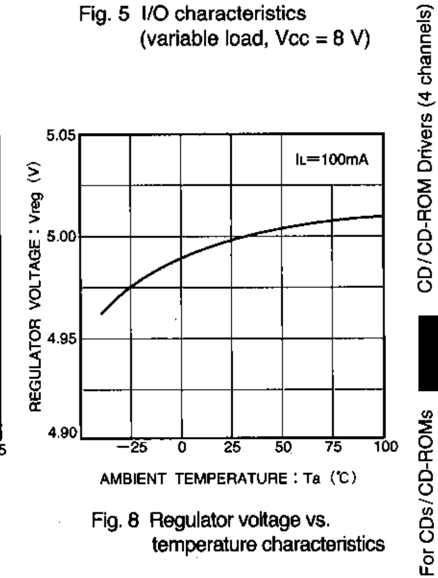


Fig. 8 Regulator voltage vs. temperature characteristics

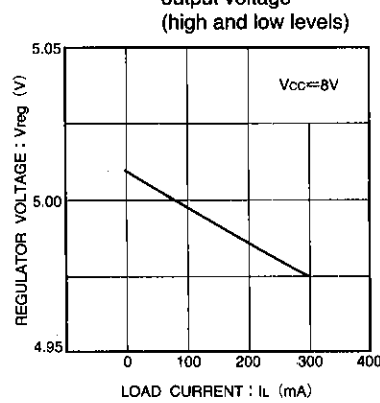


Fig. 9 Load current vs. regulator voltage

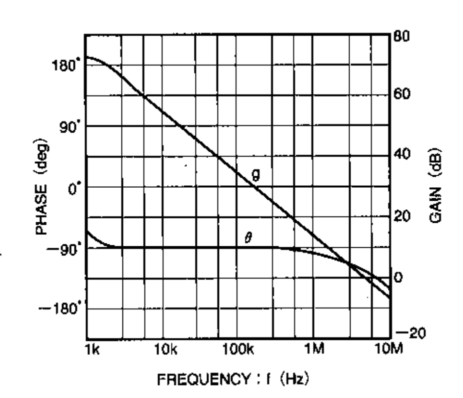
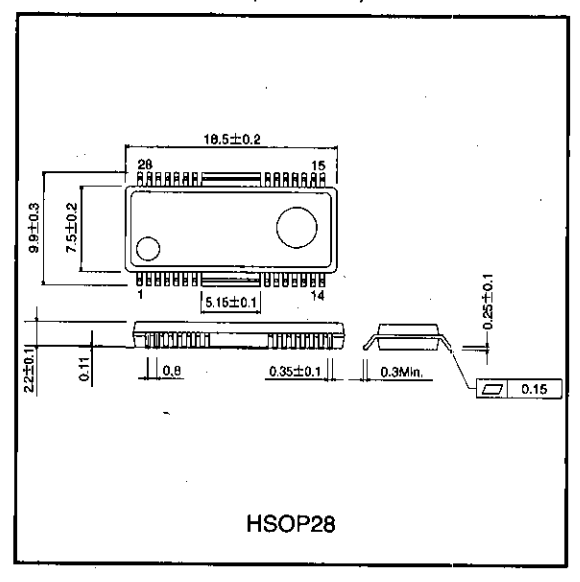


Fig. 10 Operational amplifier vs. open loop characteristics

● External dimensions (Units: mm)



HSOP28